Arithmetic-aware optimal design of FIR/IIR filters

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In this presentation we overview a novel optimisation approach for hardware-aware design of LTI digital filters. The coefficient design, quantization to fixed-point representation and implementation, typically conducted independently, are now gathered into one global optimization problem, modelled through integer linear programming (ILP) and efficiently solved using generic solvers. This work targets multiplierless hardware designs, in which costly generic multiplications by constants are replaced with additions and bit-shifts, which permits to achieve low-power designs suitable for most critical embedded systems. We guarantee the frequency-domain specifications and stability (for IIR of order 2), which together with optimal number of adders needed for a multiplierless implementation will significantly simplify design-space exploration for filter designers. Since only a certain number of output bits is typically needed, internal truncations can be introduced in order to save resources. We analyze the propagation of the possible rounding errors through the filters and use just a right amount of guard bits for internal computation that guarantees a user-specified error bound, which is especially important in the feedback loop of IIR filters. The optimal filters are implemented within the FloPoCo IP core generator and synthesized for Field Programmable Gate Arrays. To demonstrate their effectiveness, we perform several experiments using established design problems from the literature, showing superior results.
The presentation is based on the results from [1, 2, 3].

[1] Florent de Dinechin, Silviu-Ioan Filip, Martin Kumm, and Anastasia Volkova. Towards arithmetic-centered filter design. In *2021 IEEE 28th Symposium on Computer Arithmetic (ARITH)*, pages 115–118, 2021.

[2] Rx00E9 ;mi Garcia, Anastasia Volkova, Martin Kumm, Alexandre Goldsztejn, and Jonas Kx00FC ;hle. Hardware-aware design of multiplierless second-order iir filters with minimum adders. *IEEE Transactions on Signal Processing*, 70 :1673–1686, 2022.

[3] Martin Kumm, Anastasia Volkova, and Silviu-Ioan Filip. Design of optimal multiplierless fir filters with minimal number of adders. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pages 1–1, 2022.

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