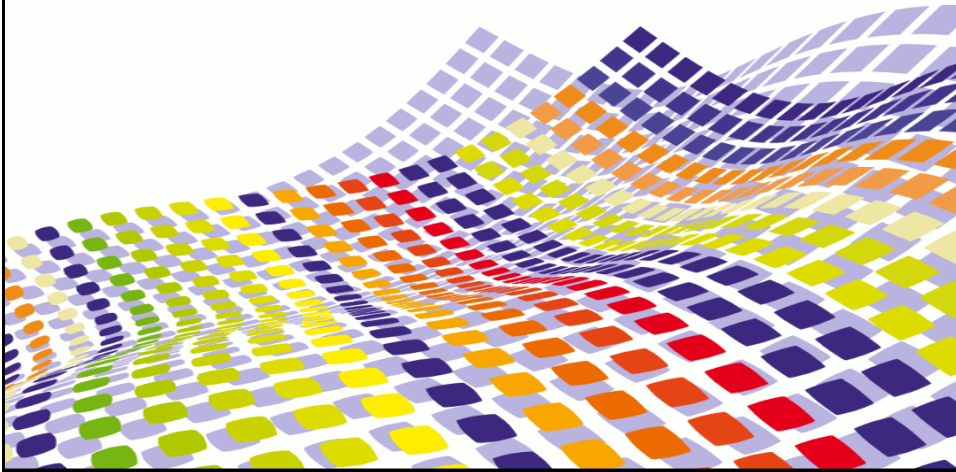



## HMPP Origins

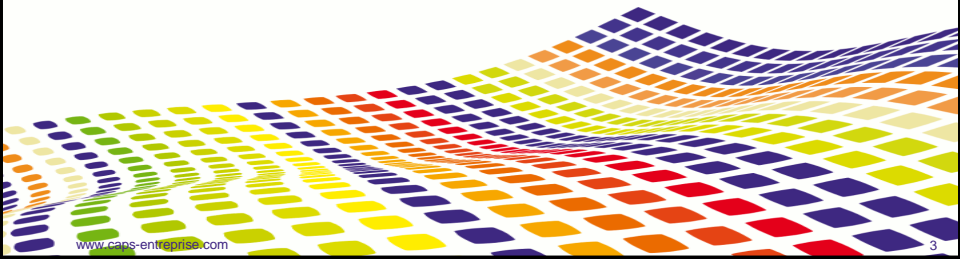


## Agenda


- GPGPU & Hybrid Parallel computing
- HMPP Concepts and Overview
- Starting with HMPP
- Addressing hardware accelerators with HMPP
- HMPP Toolchain
- HMPP Runtime
- Managing Data with HMPP
- Grouping Codelets
- Sharing Data with HMPP
- HMPP Features & Roadmap



# GPGPU & Parallel Hybrid Computing

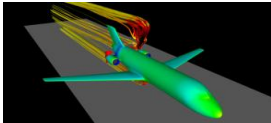


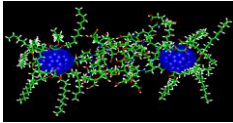
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## Industry and Business Facts

- Modeling & Simulation are pervasive

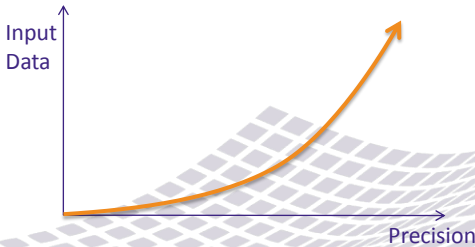






- Precision is the key to success

Input Data



Precision

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## Why Hybrid Computing?

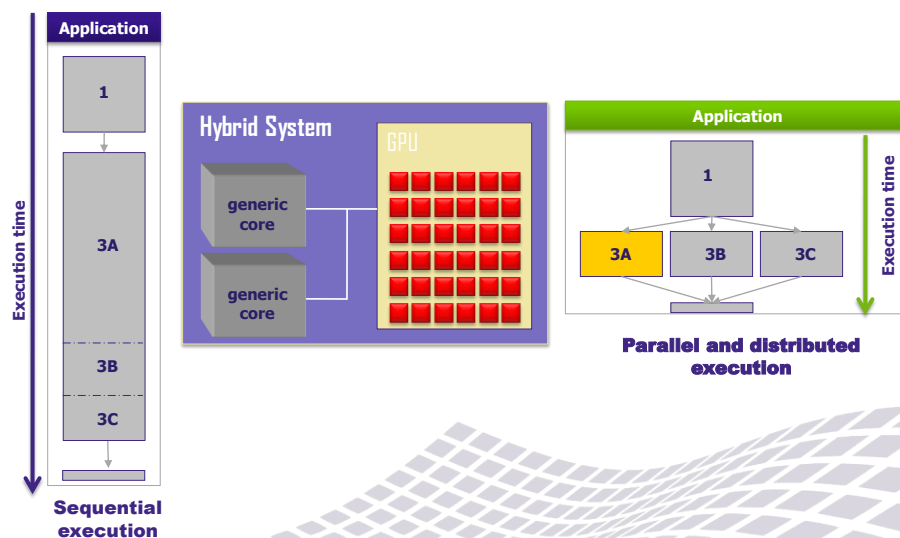


- More precision implies more data to process
  - But still in the same time, so more speed in computations!
- Current technologies reached a limit (in terms of frequency)
- One solution is to use parallelism (increase # of cores)
  - We do more things in parallel instead of doing it quicker
- The efficiency scale evolves according economic issues
  - Performance / Power consumption
  - Performance / Development time
  - ...
- Mainstream applications will rely on these multicore / manycore architectures
- Various heterogeneous hardware
  - General purpose cores
  - Application specific cores (e.g. GPUs)

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## You said Parallel Hybrid Application?



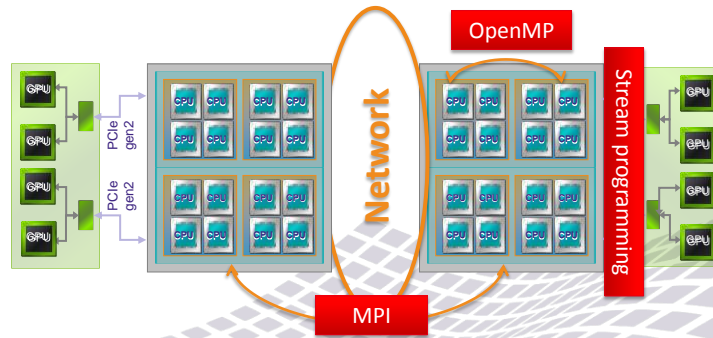
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## Multiple Parallelism Levels



- Adding a new layer of specific hardware is adding a new workload to the developer
- Programming various hardware components of a node cannot be done separately



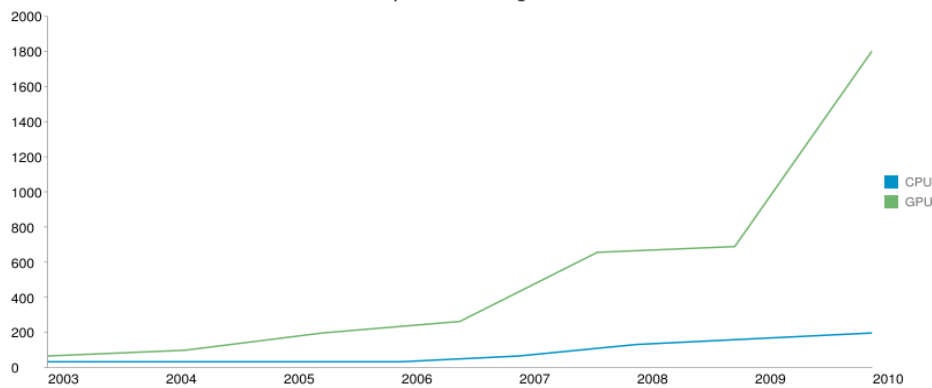
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## Parallel Processor Architectures



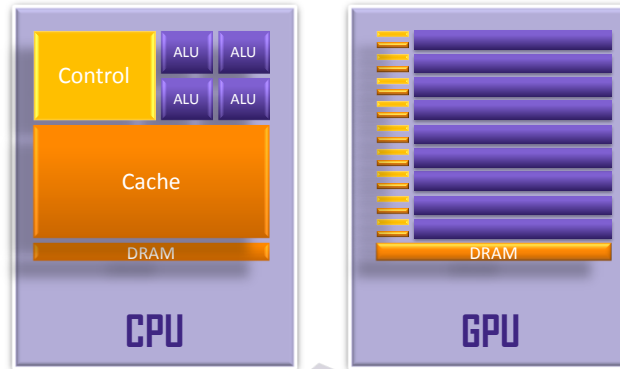
Peak performance growth



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## Parallel Processor Architectures



General purpose architecture

Massively data parallel

Needs 1000s of computation threads  
to be efficient

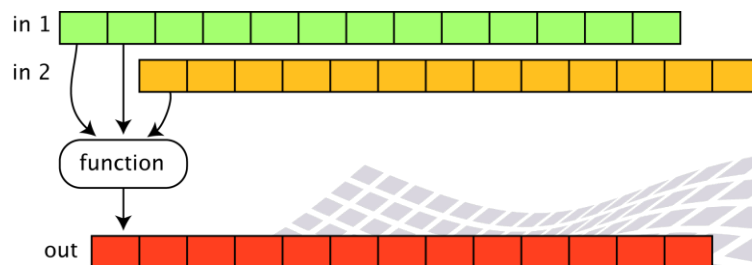
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## Stream computing



- Stream programming is well suited to GPU
  - But memory hierarchy is exposed
- A similar computation is performed on a collection of data (*stream*)
  - There is no data dependence between the computation on different stream elements



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## Offloading computations



- **Host: General purpose cores**
  - Share a main memory
  - Core ISA provides fast SIMD instructions
- **Device: Streaming cores**
  - GPU, DSP, FPGA... (vector, SIMD)
  - Application specific architectures
  - Can be extremely fast
- **Hundreds of GigaOps**
  - But not easy to leverage
  - Restriction to one platform is not acceptable

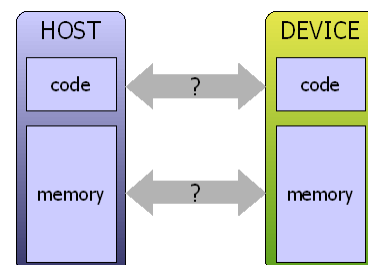
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## Key Issues



- Using accelerators makes you stick to a proprietary language/environment/technology
- **Huge potential performance but accelerators are far from host memory**
  - Data must be copied on the remote device
  - Due to narrowband links between CPU/HWA, data transfers are critical
- Therefore rethink the computation organization/algorithm



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